What is claimed is:

1. A lead frame comprising:

a stage for mounting a semiconductor chip thereon;

a plurality of groups of leads arranged in a periphery of the stage;

a plurality of lead interconnection members for interconnecting a plurality of leads in each group of the leads respectively; and

a hollow that is formed to concave in a thickness direction on each lead, thus allowing a plurality of cutting lines to pass therethrough,

wherein the plurality of lead interconnection members and the plurality of leads are subjected to cutting at the cutting lines so that the plurality of leads are made electrically independent of each other.

2. A lead frame comprising:

a stage for mounting a semiconductor chip thereon;

a plurality of groups of leads arranged in a periphery of the stage;

a plurality of lead interconnection members for interconnecting a plurality of leads in each group of the leads respectively; and

a hollow that is formed to concave in a thickness direction on each lead interconnection member across the plurality of leads, thus allowing a plurality of cutting lines to pass therethrough,

wherein the plurality of lead interconnection members and the plurality of leads are subjected to cutting at the cutting lines so that the plurality of leads are made electrically independent of each other.

3. A manufacturing method for a semiconductor package comprising the steps of:

forming a lead frame by processing a thin metal plate, wherein the lead frame comprises a stage for mounting a semiconductor chip thereon, a plurality of groups of leads arranged in a periphery of the stage, and a plurality of lead interconnection members for interconnecting a plurality of leads in each group of the leads respectively;

mounting the semiconductor chip on the stage of the lead frame via bonding, wherein the semiconductor chip is wired with the plurality of leads;

forming a molded resin for integrally fixing the semiconductor chip, the stage, and the leads therein;

plating prescribed surfaces of the leads that are exposed to an exterior of the molded resin; and

cutting the plurality of leads at a plurality of cutting lines so that the plurality of leads are made electrically independent of each other,

wherein a hollow is formed to concave in a thickness direction of the lead frame on each lead so as to allow the plurality of cutting lines to pass therethrough, and wherein the through holes are formed at a selected timing within a time period after the lead frame is formed and before the plating is performed on the leads.

4. A manufacturing method for a semiconductor package comprising the steps of:

forming a lead frame by processing a thin metal plate, wherein the lead frame comprises a stage for mounting a semiconductor chip thereon, a plurality of groups of leads arranged in a periphery of the stage, and a plurality of lead interconnection members for interconnecting a plurality of leads in each group of the leads respectively;

mounting the semiconductor chip on the stage of the lead frame via bonding, wherein the semiconductor chip is wired with the plurality of leads;

forming a molded resin for integrally fixing the semiconductor chip, the stage, and the leads therein;

plating prescribed surfaces of the leads that are exposed to an exterior of the molded resin; and

cutting the plurality of leads at a plurality of cutting lines so that the plurality of leads are made electrically independent of each other,

wherein a hollow is formed to concave in a thickness direction of the lead frame on each lead interconnection member so as to allow the plurality of cutting lines to pass therethrough, and wherein the through holes are formed at a selected timing within a time period after the lead frame is formed and before the plating is performed on the leads.

5. A semiconductor package having a plurality of leads that are exposed to an exterior of a molded resin, wherein a side surface of the lead is associated with a plated surface and a cut surface that adjoins the plated surface and that makes the adjacent leads to be electrically independent of each other.

6. The semiconductor package according to claim 5, wherein a backside of the lead subjected to plating is formed in a same plane together with a lower surface of the molded resin.

7. The lead frame according to claim 2, wherein each of the leads has a projecting portion that is projected inwardly into the through hole.

8. The lead frame according to claim 1, wherein the hollow is replaced with a through hole.

9. The lead frame according to claim 2, wherein the hollow is replaced with a through hole.

10. The manufacturing method for a semiconductor package according to claim 3, wherein the hollow is formed by etching.

11. The manufacturing method for a semiconductor package according to claim 4, wherein the hollow is formed by etching.